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ON

METHOD AND APPARATUS FOR EXPOSING PRE-DIFFUSED IP BLOCKS IN A SEMICONDUCTOR DEVICE FOR PROTOTYPING BASED ON HARDWARE EMULATION

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METHOD AND APPARATUS FOR EXPOSING PRE-DIFFUSED IP BLOCKS IN A SEMICONDUCTOR DEVICE FOR PROTOTYPING BASED ON HARDWARE EMULATION

FIELD OF THE INVENTION

[0001] This invention relates generally to the field of integrated circuit design, and particularly to a method and apparatus for exposing pre-diffused IP blocks in a semiconductor device for prototyping based on hardware emulation.

BACKGROUND OF THE INVENTION

[0002] Representing the internal SOC (system-on-chip) interface for the purpose of emulation is generally done by exposing one or more of the internal SOC buses, allowing system engineers to extend the emulation part utilizing external FPGA (field programmable gate array). While this approach is useful for most of the cases, it does not allow exposure of all the required interfaces for a complete and accurate emulation. Due to a limited pin count, a majority of the IC designs allow only some of the interfaces to be exposed (or some of the interfaces may be multiplexed into a unified exposed interface).

[0003] To overcome the shortcomings of limited interface exposure via the emulation device I/O, and to verify a designed circuit more accurately, prototyping technologies based on hardware emulation for verifying a designed circuit are highly pursued because hardware emulation is closer to the actual digital circuit. In a general prototyping system based on hardware emulation, the digital circuit for verification may be implemented in the prototyping engine which is composed by interconnecting reusable field programmable devices (RFPDs) and other discrete devices such as microprocessors, digital signal processors, application specific non-memory devices or memories. A RFPD includes FPGA, programmable logic device (PLD), and the like. RFPDs have been frequently used in prototyping since a digital circuit may be implemented in the

RFPDs by being simply programmed onto the RFPDs, and further, the RFPDs may be reused.

[0004] Recently a semiconductor device called "slice" (e.g., RapidSlice™ developed by LSI Logic Corporation, and the like) has been developed. A slice is a pre-manufactured chip in which all silicon layers have been built, leaving the metal layers to be completed with the customer's unique IP (intellectual property). The slice may include pre-diffused IP blocks such as memory, microprocessors, PCI-X controllers, and the like that suit the slice to a given target market, and an area of customizable logic where the customer logic may be implemented using the metal layers. A shell, i.e., some logic infrastructure, may personalize one or more pre-diffused IP blocks as an IP Subsystem. Such an IP subsystem may represent an integrated design, which includes one or more pre-diffused IP blocks and the associated shell. Each subsystem of the slice may have a SOC interface that permits the designer to interface and utilize the subsystem as part of the area of customizable logic.

[0005] A slice may enhance the efficiency of IC design since the slice may provide a designer with ready-made pre-diffused IP blocks in the slice. For example, when an IC designer needs to include an ARM microprocessor in a product, the designer may prefer to utilize a ready-made pre-diffused ARM microprocessor in a slice for prototyping rather than incorporating such an ARM microprocessor within the customized logic. However, there is a practical difficulty in this approach because the pre-diffused IP blocks (e.g., the ARM microprocessor) in the slice are typically not exposed for prototyping—the interface pins of the pre-diffused IP blocks are not normally accessible form outside the slice.

[0006] Therefore, it would be desirable to provide a method and apparatus for exposing all required pre-diffused IP blocks or IP subsystems, in a semiconductor device for the purpose of accurate prototyping based on hardware emulation.

SUMMARY OF THE INVENTION

[0007] Accordingly, the present invention is directed to a method and apparatus for exposing pre-diffused IP blocks in a semiconductor device for prototyping based on hardware emulation. According to an exemplary aspect of the present invention, multiple interfaces may be provided through shared I/O pins by selecting specific multiplexer configurations through configuration pins. A pre-diffused IP with internal SOC interfaces may be exposed by routing it to a shared pin multiplexer and may be selected for exposure by selecting a specific multiplexer configuration pins. In the event that such pre-diffused IP interfaces outside of the chip through a dedicated I/O pins, such pins may still be shared with other interfaces that require exposure. Through controlling the signals on the configuration pins and thus controlling the multiplexers currently usable I/O, any single pre-diffused IP blocks or any combination of the pre-diffused IP blocks in the semiconductor device may be exposed through corresponding I/O pins for prototyping.

[0008] In order to overcome the limited number of I/Os of such emulation device, different multiplexer configurations may expose part of the pre-diffused IP, but by utilizing all possible multiplexer configurations, all the pre-diffused IP and/or available IP subsystems may be exposed to allow full utilization of all the available IP on the slice for the purpose of prototyping. As such, one instance or multiple instances of the same emulations device, each instance being configured differently through the multiplexer configurations pins, may allow such accurate emulation.

[0009] It is to be understood that both the foregoing general description and the following detailed description are exemplary and explanatory only and are not restrictive of the invention as claimed. The accompanying drawings, which are incorporated in and constitute a part of the specification, illustrate an embodiment of the invention and together with the general description, serve to explain the principles of the invention.

BRIEF DESCRIPTION OF THE DRAWINGS

[0010] The numerous advantages of the present invention may be better understood by those skilled in the art by reference to the accompanying figures in which:

FIG. 1 is a schematic diagram of an exemplary semiconductor device in which the present invention may be implemented; and

FIG. 2 is a schematic diagram illustrating an exemplary embodiment of the present invention, wherein four semiconductor devices are connected to two FPGAs for prototyping.

DETAILED DESCRIPTION OF THE INVENTION

[0011] Reference will now be made in detail to the presently preferred embodiments of the invention, examples of which are illustrated in the accompanying drawings.

[0012] Referring first to FIG. 1, a schematic diagram of an exemplary semiconductor device 100 in which the present invention may be implemented is shown. The semiconductor device 100 may be a test chip or emulation part made based on an available slice. A slice is a pre-manufactured chip in which all silicon layers have been built, leaving the metal layers to be completed with the customer's unique IP. The semiconductor device 100 may include pre-diffused IP blocks such as a microprocessor, a ROM, a PCI-X controller, and the like. A shell, i.e., some logic infrastructure, may personalize one or more pre-diffused IP blocks as an IP subsystem. An IP subsystem may represent an integrated design, which includes one or more pre-diffused IP blocks and the associated shell. As shown in FIG. 1, the semiconductor device 100 may include IP subsystems 120, 122, 124, 126, and 128. Each IP subsystem may include one or more pre-diffused IP blocks on the slice. For example, the IP subsystem 124 may include pre-diffused IP blocks 160, 162, 164, and 168, and the IP subsystem 126 may include pre-diffused IP blocks 150, 152, 154, 156, and 158. The semiconductor device 100 may include an area of customizable logic 130. The area of customizable logic 130 may be a

sea-of-gates structure whose function may be defined by the customer. Each IP subsystem 120, 122, 124, 126, or 128 may have a system-on-chip (SOC) interface that permits the IP subsystem to interface with the area of customizable logic 130.

[0013] The semiconductor device 100 may further include configuration pins 102, 104, 106, 108, 110, 112, 114, and 116 around its four corners, and input/out (I/O) pins 118 on its four sides. The I/O pins 118 may provide input and output for the semiconductor device 100.

[0014] The present invention is directed to a method and apparatus for exposing pre-diffused IP blocks in a semiconductor device for prototyping based on hardware emulation. As shown in FIG. 1, the semiconductor device 100 may include multiple 2-input multiplexers on its four sides. A 2-input mutiplexer may have its input ports connected to interface pins of two different pre-diffused IP blocks, or IP subsystems, and its output port connected to an I/O pin. Configurations pins, one or more, may be used to select which of the input signals appears at the I/O pin. Thus, through controlling the signals ("0" or "1") on the configuration pins, which interface pin of the two IP blocks is actually connected to the I/O pin may be controlled, that is, which of the two IP blocks may be exposed to prototyping through the I/O pin may be controlled.

[0015] As shown in FIG. 1, for example, a configuration pin 108 may be provided to multiplexers 170, 172, and 174. The multiplexer 170 may be connected to an interface pin of the IP block 156 and an interface pin of the IP block 162 and output at an I/O pin 180. The multiplexer 172 may be connected to an interface pin of the IP block 158 and an interface pin of the IP block 164 and may output at an I/O pin 182. The multiplexer 174 may be connected to an interface pin of the IP block 150 and an interface pin of the IP block 168 and may output at an I/O pin 184. When the signal on the configuration pin 108 is "1" ("high"), the multiplexer 170 may output the signals on the interface pin of the IP block 156 at the I/O pin 180, the multiplexer 172 may output the signals on the

interface pin of the IP block 158 at the I/O pin 182, and the multiplexer 174 may output the signals on the interface pin of the IP block 150 at the I/O pin 184. Thus, when the signal on the configuration pin 108 is "1" ("high"), the IP blocks 156, 158, and 150 may be exposed for prototyping, that is, the IP blocks 156, 158, and 150 may interface directly with RFPDs (not shown in FIG. 1, but see FIG. 2) through the I/O pins 180, 182, 184, respectively. Alternately, when the signal on the configuration pin 108 is "0" ("low"), the multiplexer 170 may output the signals on the interface pin of the IP block 162 at the I/O pin 180, the multiplexer 172 may output the signals on the interface pin of the IP block 164 at the I/O pin 182, and the multiplexer 174 may output the signals on the interface pin of the IP block 168 at the I/O pin 184. Thus, when the signal on the configuration pin 108 is "0" ("low"), the IP blocks 162, 164, and 168 may be exposed for prototyping, that is, the IP blocks 162, 164, and 168 may interface directly with RFPDs (not shown in FIG. 1, but see FIG. 2) through the I/O pins 180, 182, 184, respectively.

[0016] Those of ordinary skill in the art will understand that using configuration pins to provide addresses to multiplexers and thus to control the output/input of multiplexers, any single pre-diffused IP blocks or any combination of the pre-diffused IP blocks and/or IP subsystems in the semiconductor device 100 may be exposed through corresponding I/O pins for prototyping.

[0017] It is understood that FIG. 1 is intended as an example of a semiconductor device in which the present invention may be implemented and not as an architectural limitation to the present invention. Those of ordinary skill in the art will appreciate that various combinations and arrangements may be employed without departing from the scope and spirit of the present invention. For example, although multiplexers shown in FIG. 1 have two inputs, multiplexers with three or more inputs may also be used without departing from the scope and spirit of the present invention. Additionally, the positions of configurations pins may not necessarily be around the corners of the semiconductor device.

[0018] FIG. 2 is a schematic diagram illustrating an exemplary embodiment of the present invention, wherein four semiconductor devices 202, 204, 206, and 208 are connected to two FPGAs 210 and 212 for prototyping. The semiconductor devices 202, 204, 206, and 208 may be slices and may have same or similar internal structure (not shown in FIG. 2) as the semiconductor device 100. Specifically, each of the semiconductor devices 202, 204, 206, and 208 may have pre-diffused IP blocks and an area of customizable logic. Each of the semiconductor devices 202, 204, 206, and 208 may have configuration pins around its four corners, and input/out (I/O) pins on its four sides for providing input and output for the semiconductor device, and multiplexers on its four sides. A mutiplexer may have its input ports connected to interface pins of different pre-diffused IP blocks and its output port connected to an I/O pin. A binary address may be used to select which of the input signals appears at the I/O pin. The binary address may be provided through a configuration pin, which is communicatively coupled to the mutiplexer. Thus, through controlling the signal on the configuration pin which provides an address to the mutiplexer, the interface pin of the IP blocks that is actually connected to the I/O pin may be chosen, that is, the IP block that is exposed to prototyping through the I/O pin may be controlled.

[0019] Using configuration pins to provide addresses to multiplexers and thus to control the output of multiplexers, any single pre-diffused IP blocks or any combination of the pre-diffused IP blocks in the semiconductor devices 202, 204, 206, and 208 may be exposed through corresponding I/O pins for prototyping. For example, two separate pre-diffused IP blocks in the semiconductor device 202 may be simultaneously exposed for prototyping: one for the FPGA 210, and the other for FPGA 212.

[0020] It is understood that the specific order or hierarchy of steps in the methods disclosed are examples of exemplary approaches. Based upon design preferences, it is understood that the specific order or hierarchy of steps in the method can be rearranged

while remaining within the scope of the present invention. The accompanying method claims present elements of the various steps in a sample order, and are not meant to be limited to the specific order or hierarchy presented.

[0021] It is believed that the present invention and many of its attendant advantages will be understood by the foregoing description. It is also believed that it will be apparent that various changes may be made in the form, construction and arrangement of the components thereof without departing from the scope and spirit of the invention or without sacrificing all of its material advantages. The form herein before described being merely an explanatory embodiment thereof, it is the intention of the following claims to encompass and include such changes.